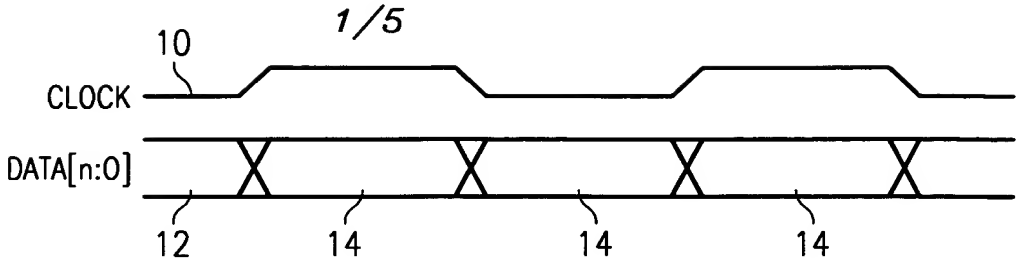
FIG. 1



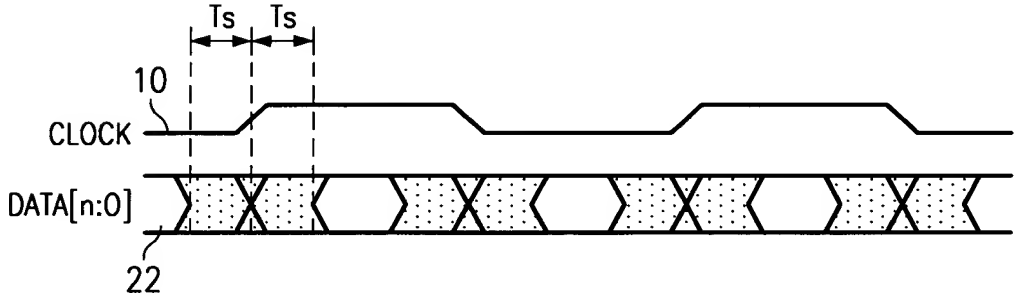


FIG. 2

FIG. 4A

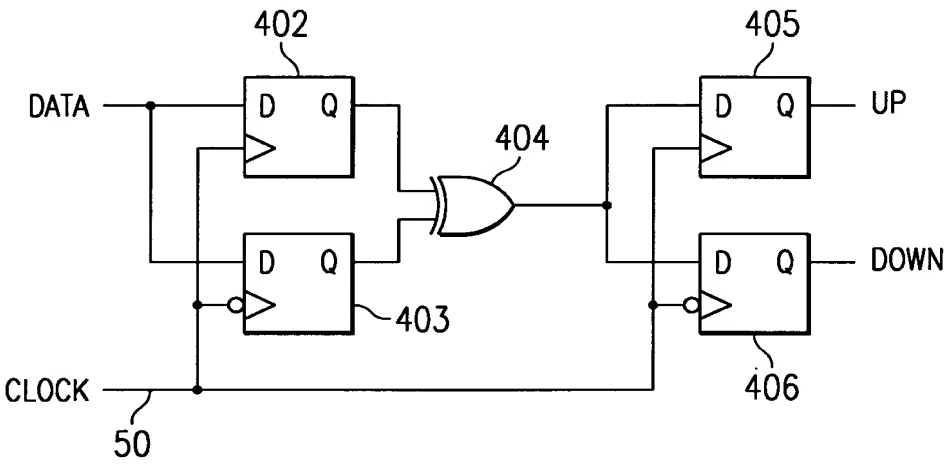


FIG. 4B

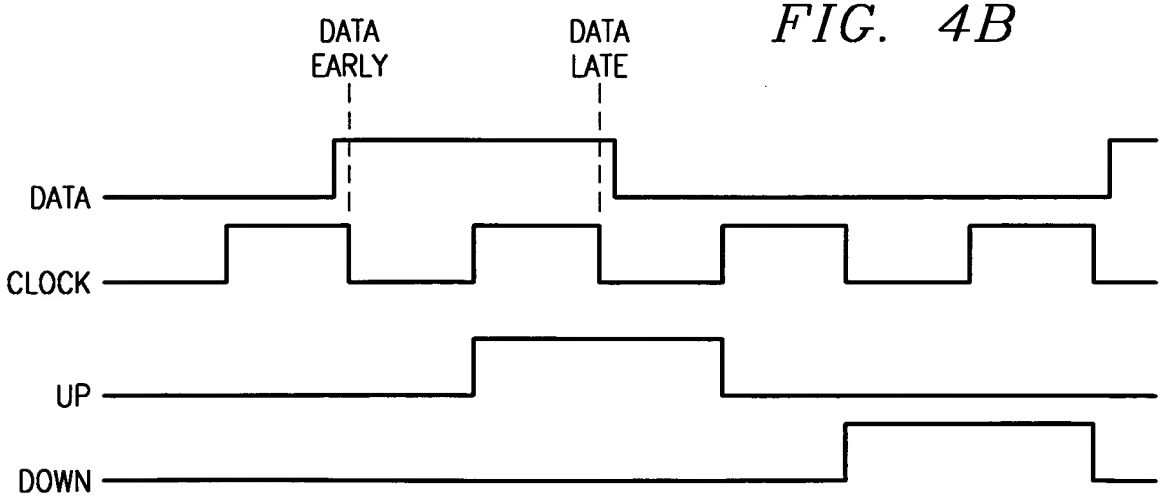


FIG. 3

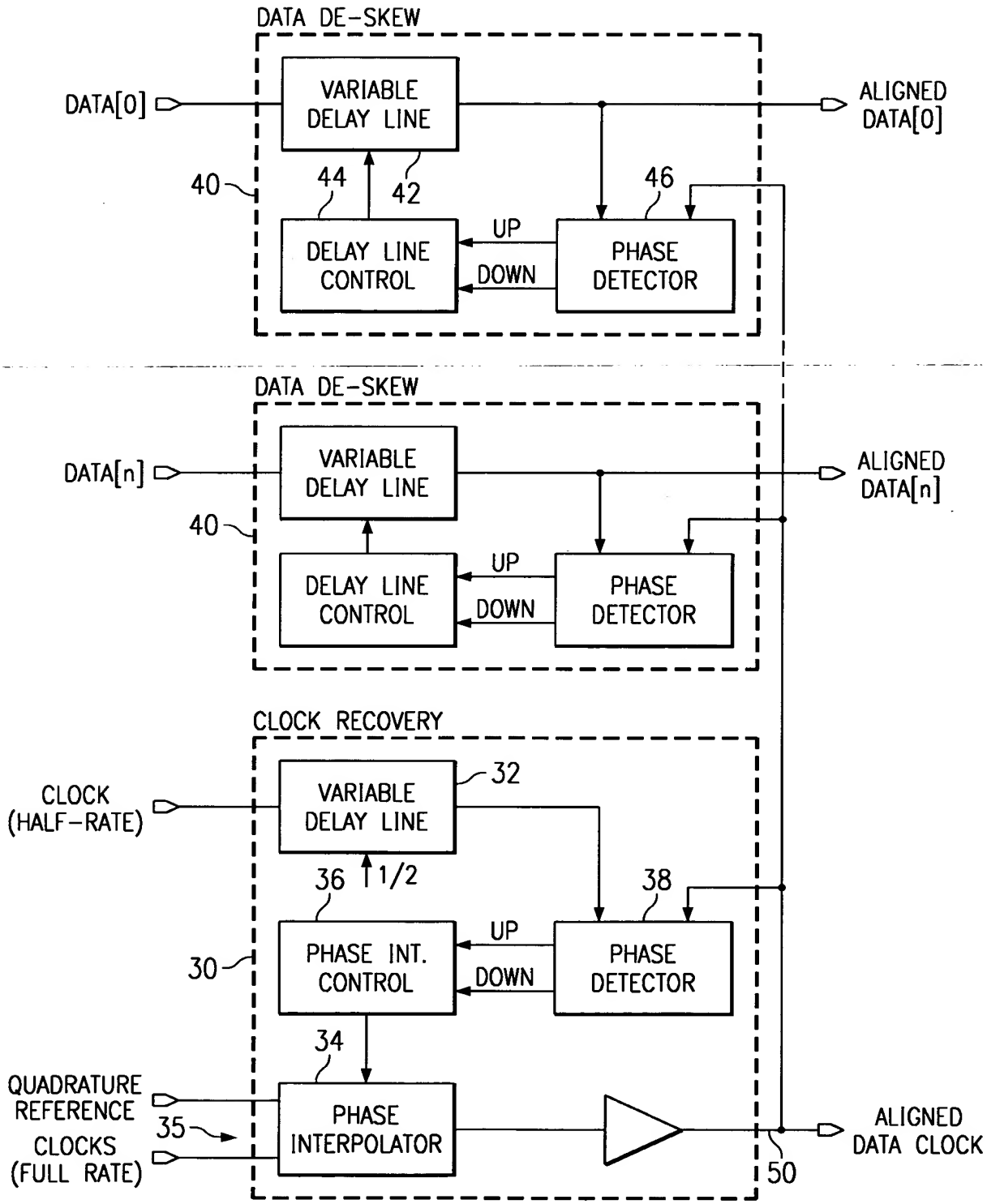

DATA DE-SKEW
DATA[0]
VARIABLE DELAY LINE
ALIGNED DATA[0]
40
44
42
46
DELAY LINE CONTROL
UP
DOWN
PHASE DETECTOR
DATA DE-SKEW
DATA[n]
VARIABLE DELAY LINE
ALIGNED DATA[n]
40
DELAY LINE CONTROL
UP
DOWN
PHASE DETECTOR
CLOCK RECOVERY
CLOCK (HALF-RATE)
VARIABLE DELAY LINE
32
36
1/2
38
30
PHASE INT. CONTROL
UP
DOWN
PHASE DETECTOR
34
QUADRATURE REFERENCE CLOCKS (FULL RATE)
35
PHASE INTERPOLATOR
ALIGNED DATA CLOCK
50

FIG. 5

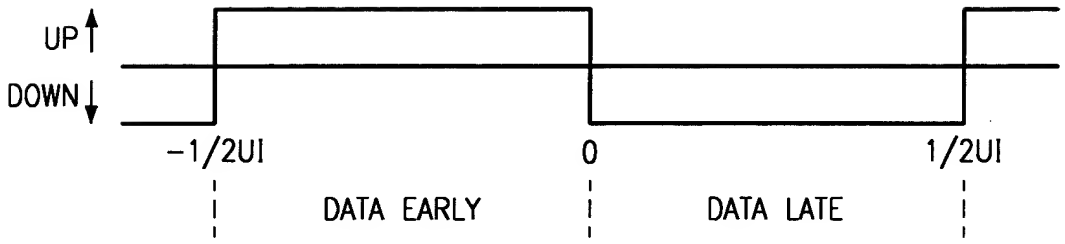


FIG. 6

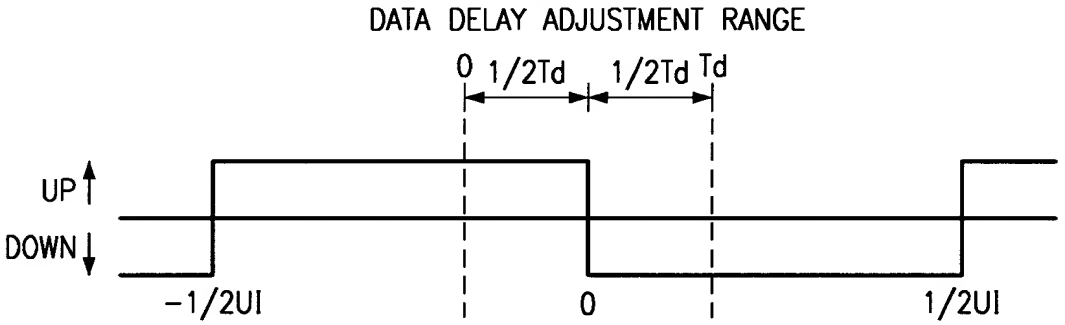


FIG. 7

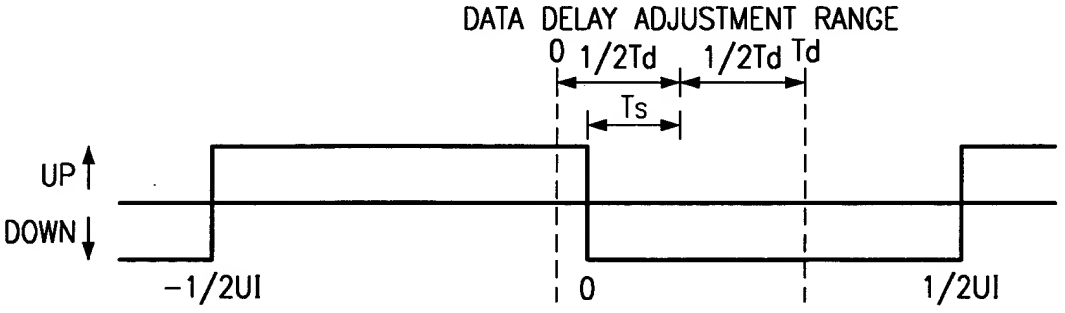
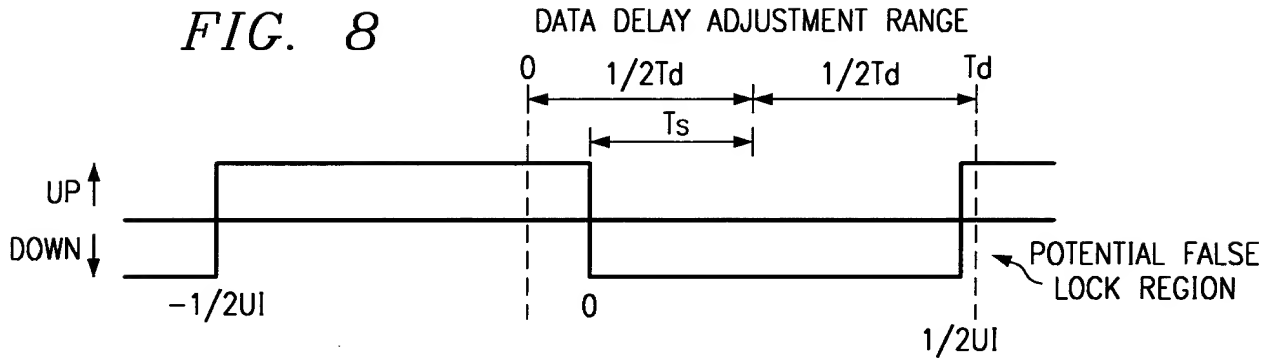


FIG. 8


DATA DELAY ADJUSTMENT RANGE
0
1/2Td
1/2Td
Td
Ts
UP
DOWN
-1/2UI
0
1/2UI
POTENTIAL FALSE
LOCK REGION

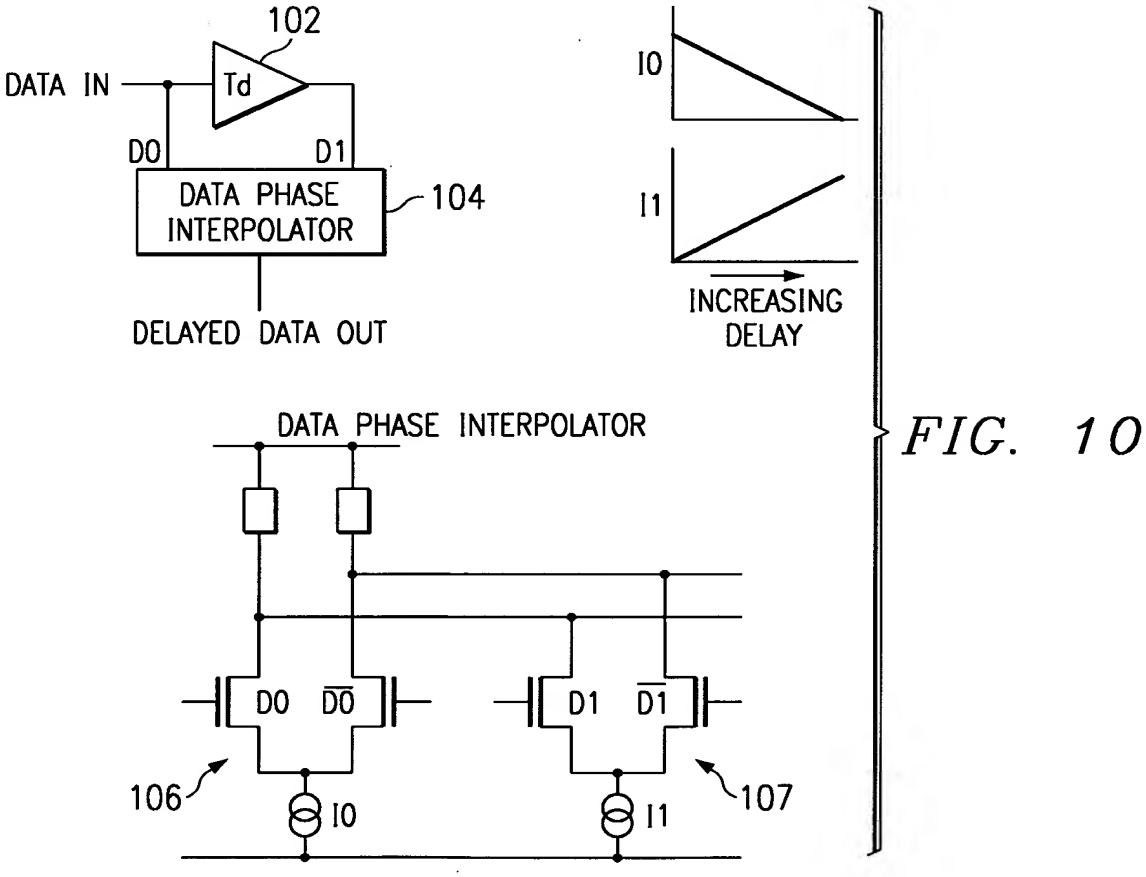
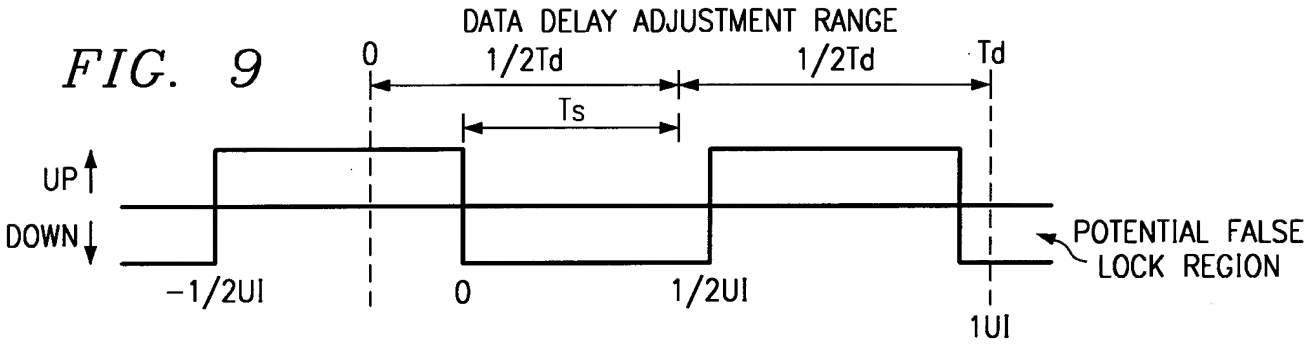

102
DATA IN
Td
D0
D1
DATA PHASE
INTERPOLATOR
104
DELAYED DATA OUT
I0
I1
INCREASING
DELAY
DATA PHASE INTERPOLATOR
D0
D0
D1
D1
106
107
I0
I1

FIG. 10

FIG. 9


DATA DELAY ADJUSTMENT RANGE
0
1/2Td
1/2Td
Td
Ts
UP
DOWN
POTENTIAL FALSE LOCK REGION
-1/2UI
0
1/2UI
1UI

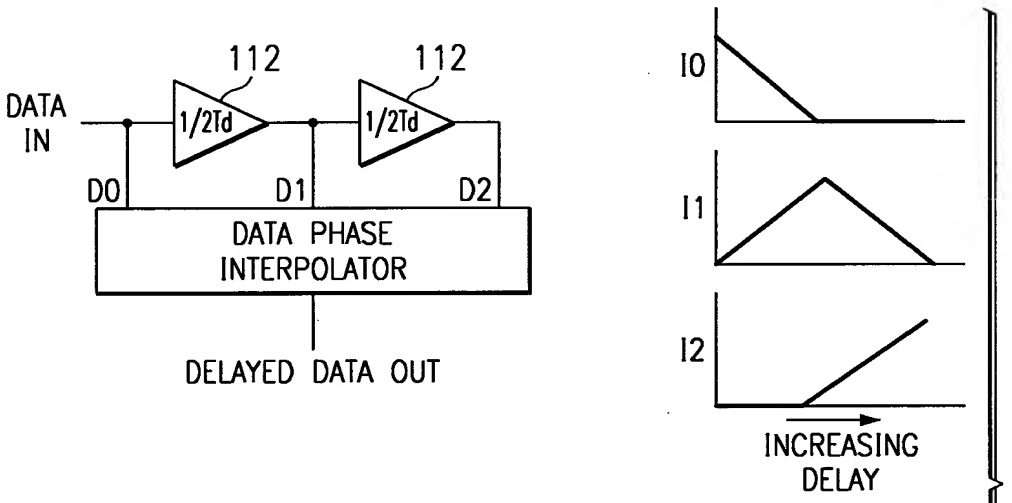
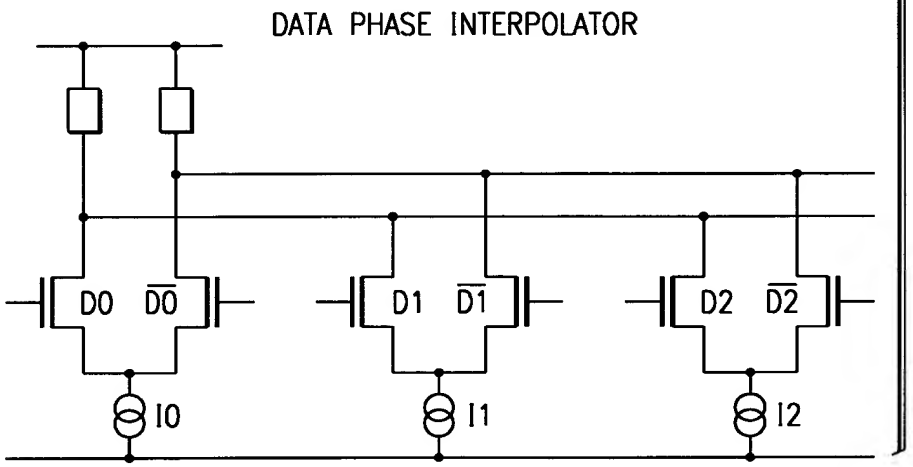

112
112
DATA IN
1/2Td
1/2Td
D0
D1
D2
DATA PHASE INTERPOLATOR
DELAYED DATA OUT
I0
I1
I2
INCREASING DELAY

FIG. 11


DATA PHASE INTERPOLATOR
D0
D0
D1
D1
D2
D2
I0
I1
I2